HGD098N10A , HGI098N10A P-1

100V N-Ch Power MOSFET

V_{DS}	100	V
$R_{DS(on),typ}$	8.8	mΩ
$I_{D\ (Sillicon\ Limited)}$	67	A

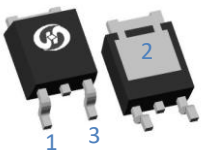
Feature

◇ High Speed Power Switching
◇ Enhanced Body diode dv/dt capability
◇ Enhanced Avalanche Ruggedness
◇ 100% UIS Tested, 100% Rg Tested
◇ Lead Free, Halogen Free

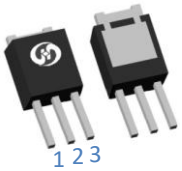
Application

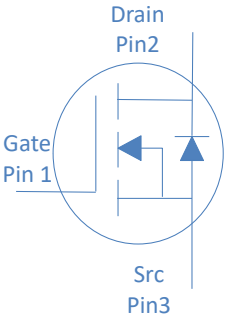
◇ Synchronous Rectification in SMPS
◇ Hard Switching and High Speed Circuit
◇ DC/DC in Telecoms and Inductrial

TO-252



TO-251





Part Number	Package	Marking
HGD098N10A	TO-252	GD098N10A
HGI098N10A	TO-251	GI098N10A

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	67	A
		T_C=100℃	48	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	190	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	31	mJ
Power Dissipation	P_D	T_C=25℃	94	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.6	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	3.0	4.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=100V, T_j=25℃	-	-	1	μA
		V_{GS}=0V, V_{DS}=100V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	8.8	9.8	mΩ
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	39	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	1326	-	pF
Output Capacitance	C_{oss}		-	262	-	
Reverse Transfer Capacitance	C_{rss}		-	7.7	-	
Total Gate Charge	Q_g(10V)	V_{DD}=50V, I_D=20A, V_{GS}=10V	-	23	-	nC
Gate to Source Charge	Q_{gs}		-	5.5	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	6.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=10Ω,	-	6	-	ns
Rise time	t_r		-	3	-	
Turn off Delay Time	$t_{d(off)}$		-	17	-	
Fall Time	t_f		-	4	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=20A, dI_F/dt=500A/μs	-	52	-	ns
Reverse Recovery Charge	Q_{rr}		-	176	-	nC

Fig 1. Typical Output Characteristics

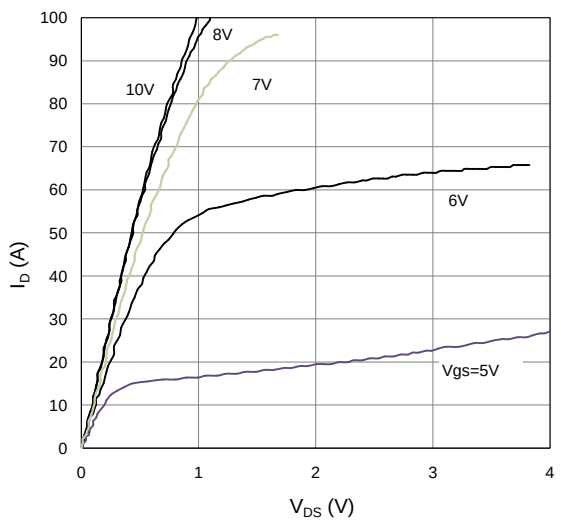


Figure 2. On-Resistance vs. Gate-Source Voltage

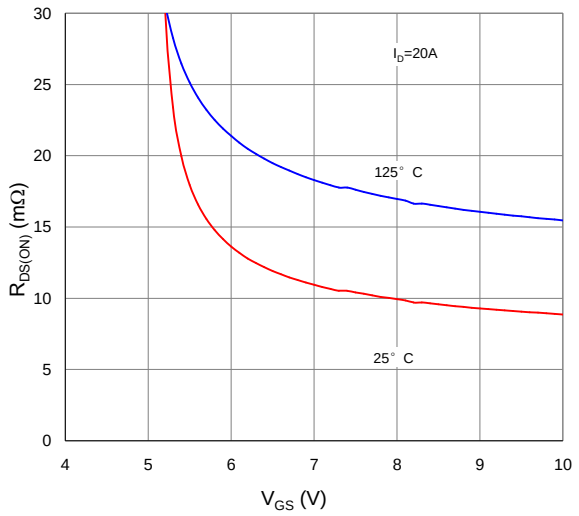


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

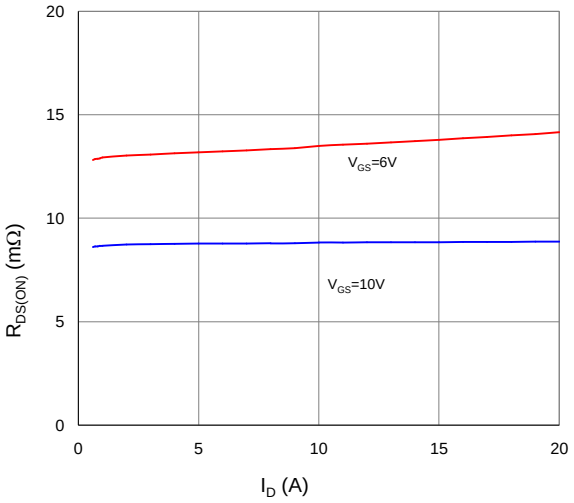


Figure 4. Normalized On-Resistance vs. Junction Temperature

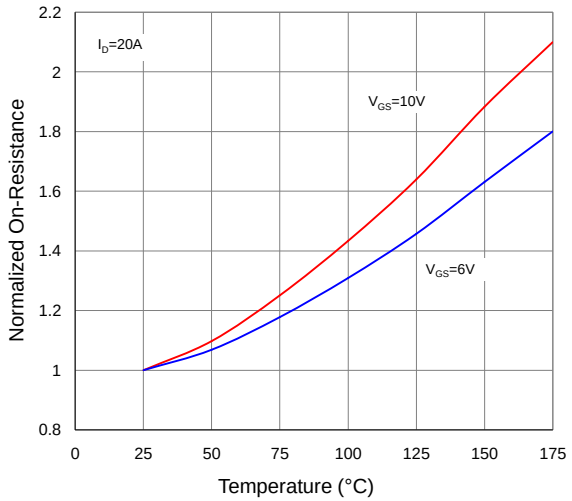


Figure 5. Typical Transfer Characteristics

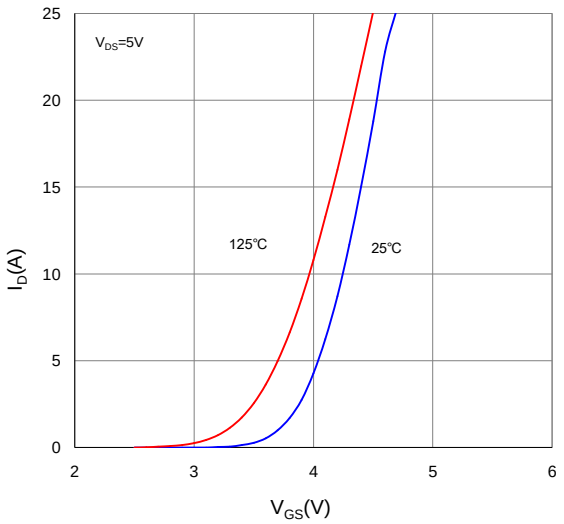


Figure 6. Typical Source-Drain Diode Forward Voltage

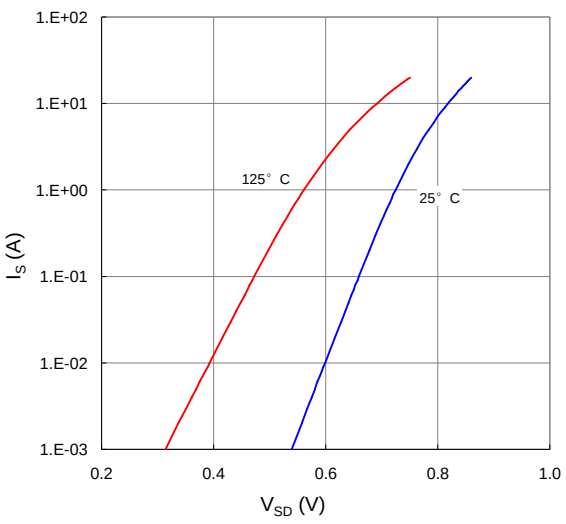


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

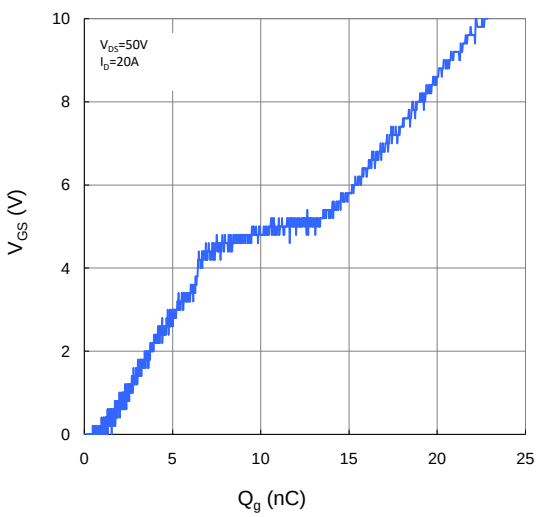


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

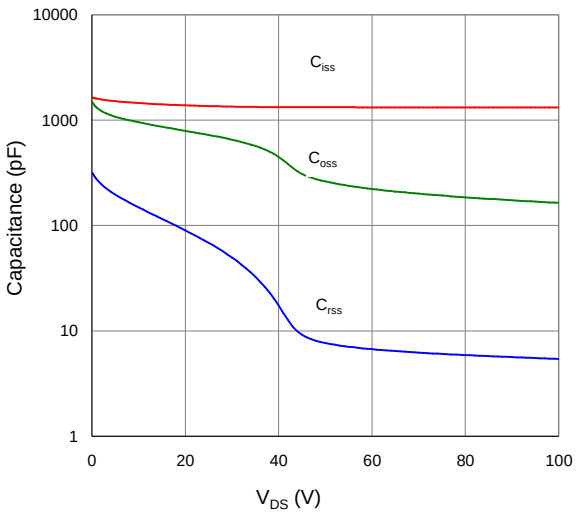


Figure 9. Maximum Safe Operating Area

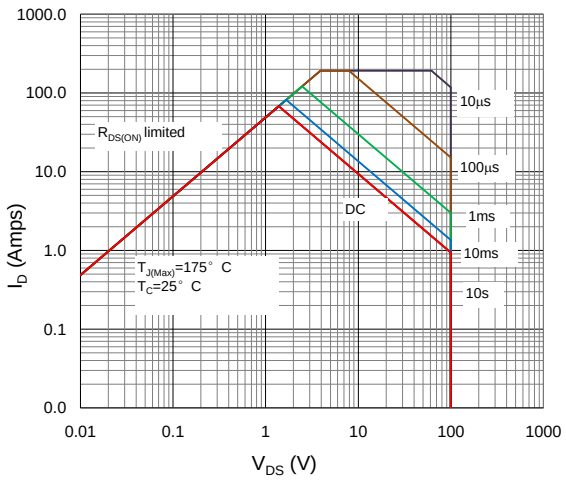


Figure 10. Maximun Drain Current vs. Case Temperature

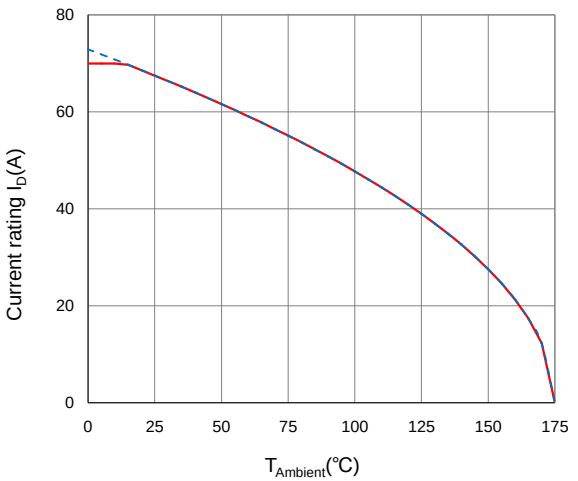
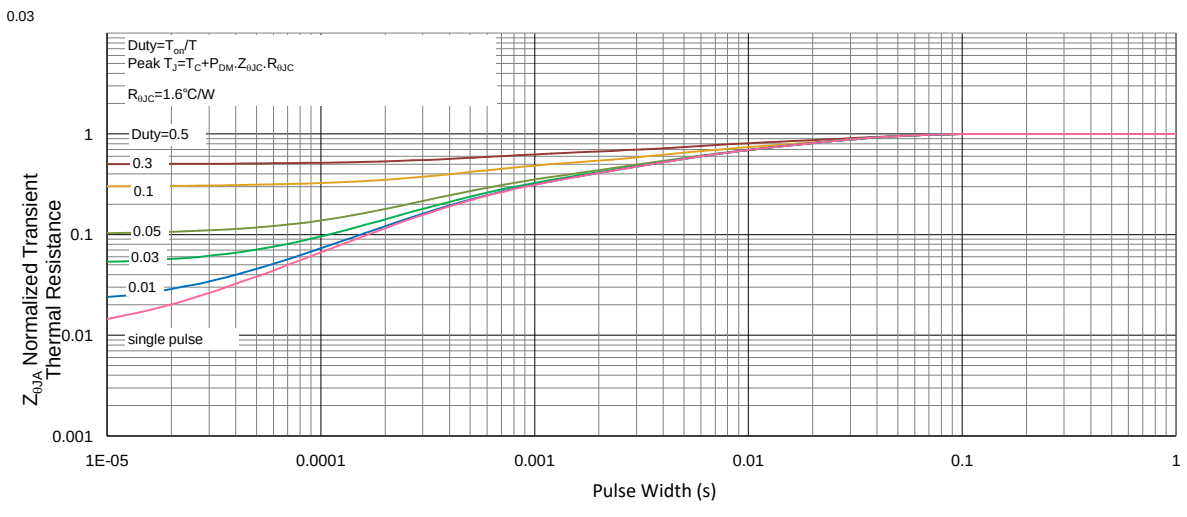
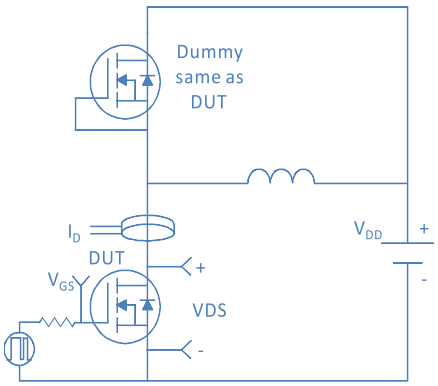
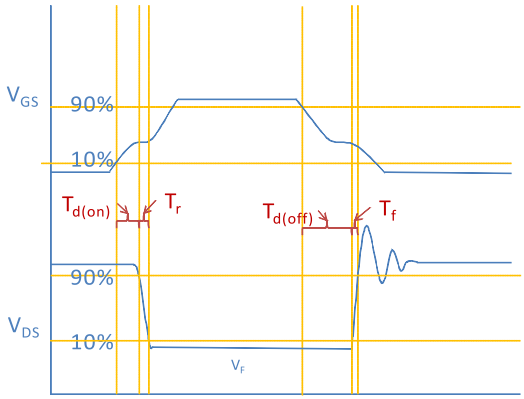


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

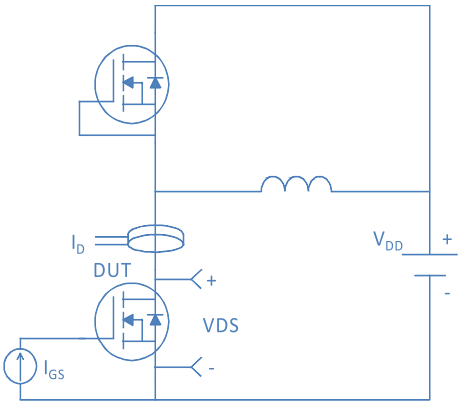


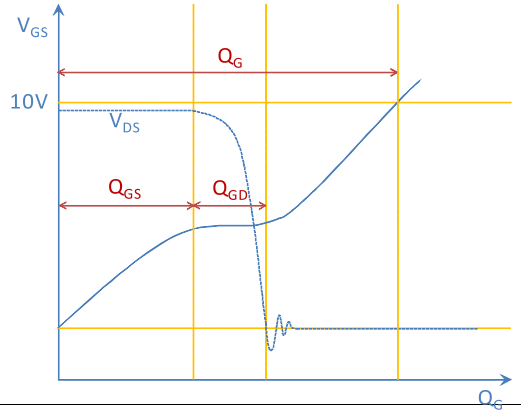
Inductive switching Test



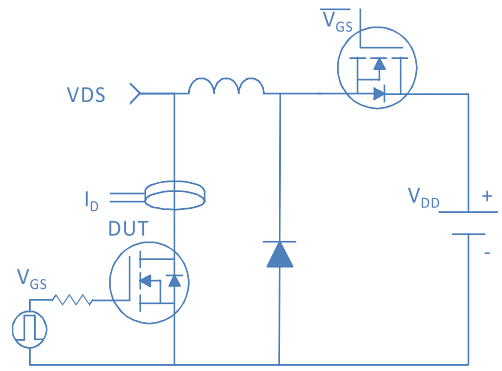


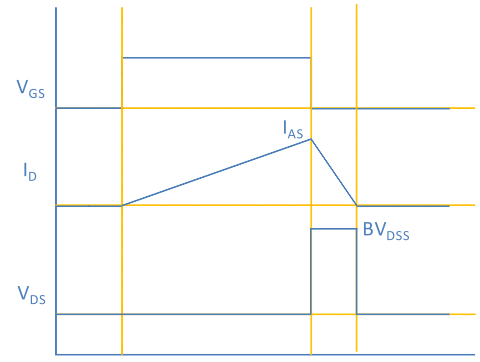
Gate Charge Test



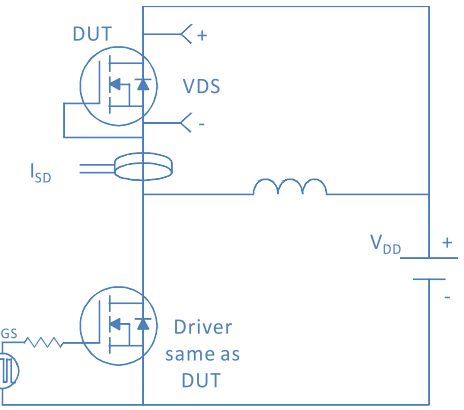


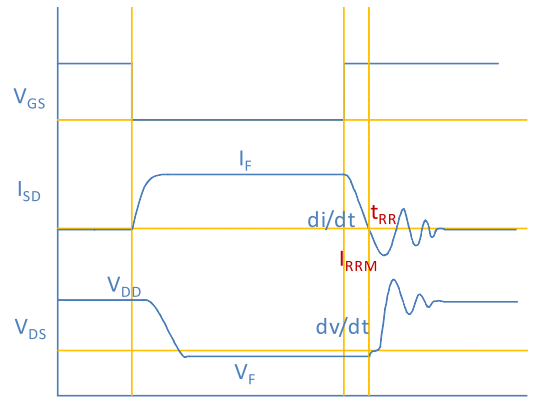
Uclamped Inductive Switching (UIS) Test





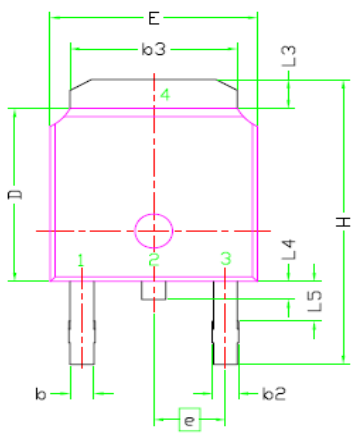
Diode Recovery Test

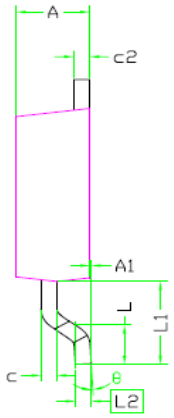




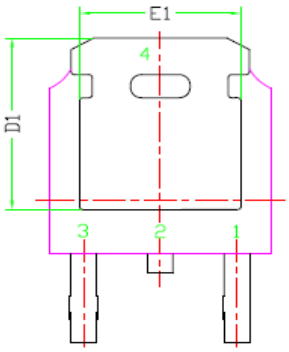
Package Outline

TO-252, 2 leads

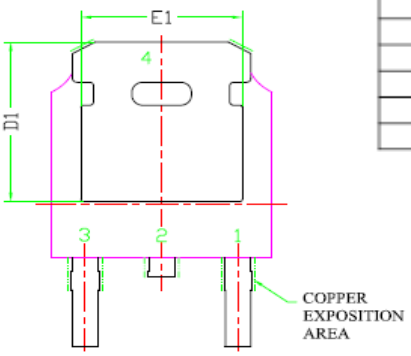




SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1		2.743 REF	
L2		0.508 BSC	
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e		2.286 BSC	
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.46	0.50	0.60
c2	0.46	0.50	0.58
D1	5.21	--	--
E1	4.40	--	--
θ	0°	--	10°



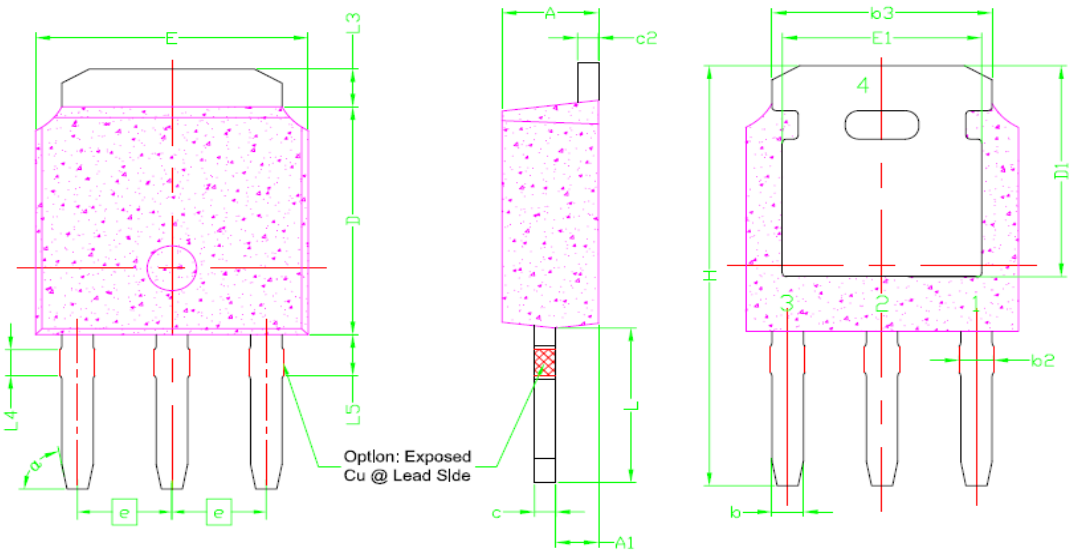
SINGLE ROW(NEW)



MATRIX L/F

Package Outline

TO-251, 3leads



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	3.98	4.13	4.28
L3	0.89	--	1.27
L4		0.698 REF	
L5	0.972	1.099	1.226
D	6.00	6.10	6.223
H	11.05	11.25	11.45
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e		2.286 BSC	
A	2.20	2.30	2.38
A1	0.89	1.04	1.15
c	0.46	0.50	0.60
c2	0.46	0.50	0.60
D1	5.10	--	--
E1	4.40	--	--
α		79° REF	