

**100V N-Ch Power MOSFET**
**Feature**

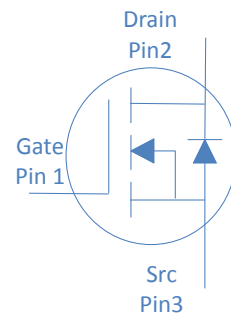
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

$V_{DS}$			100	V
$R_{DS(on),typ}$	TO-263	$V_{GS}=10V$	8.7	$m\Omega$
$R_{DS(on),typ}$		$V_{GS}=4.5V$	10.7	$m\Omega$
$R_{DS(on),typ}$	TO-220	$V_{GS}=10V$	9.0	$m\Omega$
$R_{DS(on),typ}$		$V_{GS}=4.5V$	11	$m\Omega$
$I_D$ (Silicon Limited)			73	A

**Application**

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

**TO-263**

**TO-220**


Part Number	Package	Marking
HGB110N10SL	TO-263	GB110N10SL
HGP110N10SL	TO-220	GP110N10SL

**Absolute Maximum Ratings at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ\text{C}$	73	A
		$T_C=100^\circ\text{C}$	52	
Drain to Source Voltage	$V_{DS}$	-	100	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	190	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.1\text{mH}, T_C=25^\circ\text{C}$	22	mJ
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	125	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 175	$^\circ\text{C}$

**Absolute Maximum Ratings**

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.2	$^\circ\text{C/W}$

**Electrical Characteristics at  $T_J=25^{\circ}\text{C}$  (unless otherwise specified)**
**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.4	1.9	2.4	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=100V, T_J=25^{\circ}\text{C}$	-	-	1	$\mu A$
		$V_{GS}=0V, V_{DS}=100V, T_J=100^{\circ}\text{C}$	-	-	100	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$ TO-263	-	8.7	10.7	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$ TO-263	-	10.7	13.7	
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$ TO-220	-	9	11	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$ TO-220	-	11	14	
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$	-	60	-	S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	1.5	-	$\Omega$

**Dynamic Characteristics**

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$	-	2275	-	pF
Output Capacitance	$C_{oss}$		-	162	-	
Reverse Transfer Capacitance	$C_{rss}$		-	7.9	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=50V, I_D=14A, V_{GS}=10V$	-	29	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	14	-	
Gate to Source Charge	$Q_{gs}$		-	5	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	5	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=14A, V_{GS}=10V,$ $R_G=10\Omega,$	-	8	-	ns
Rise time	$t_r$		-	3	-	
Turn off Delay Time	$t_{d(off)}$		-	26	-	
Fall Time	$t_f$		-	4	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R=50V, I_F=12A, di_F/dt=500A/\mu s$	-	33	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	157	-	nC

Figure 1. Typical Output Characteristics

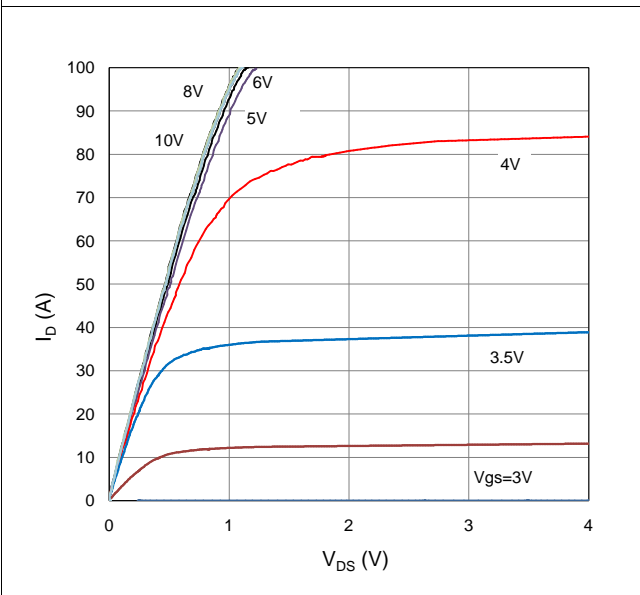


Figure 2. On-Resistance vs. Gate-Source Voltage

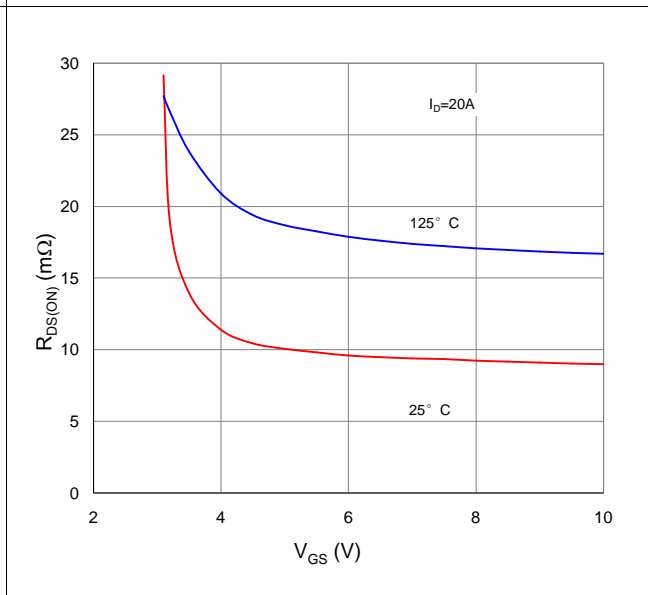


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

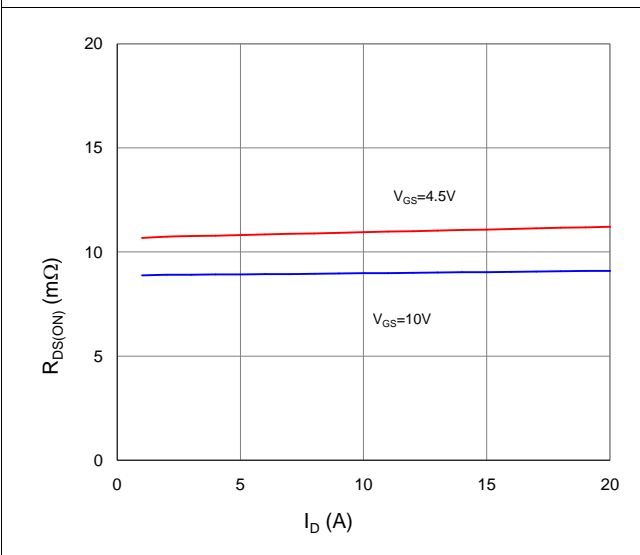


Figure 4. Normalized On-Resistance vs. Junction Temperature

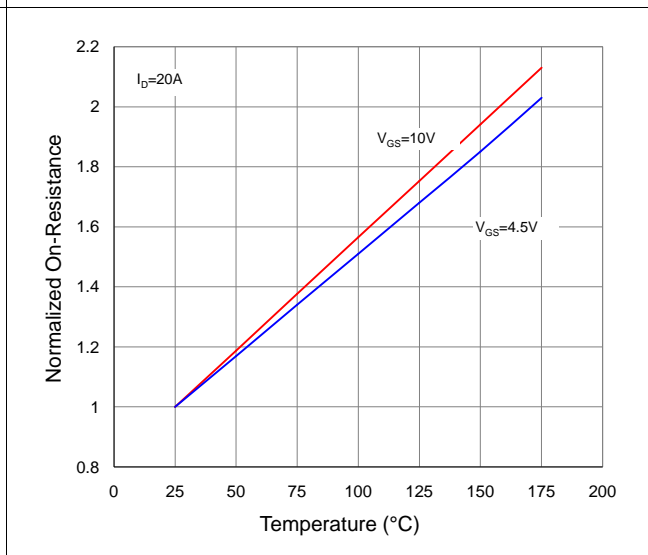


Figure 5. Typical Transfer Characteristics

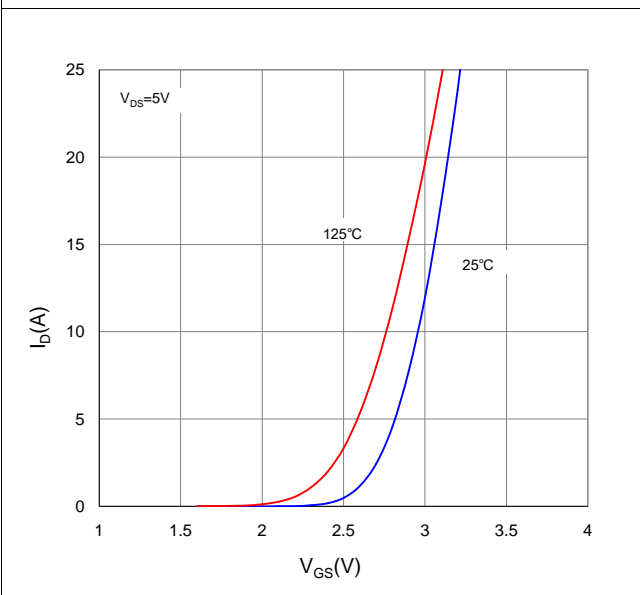


Figure 6. Typical Source-Drain Diode Forward Voltage

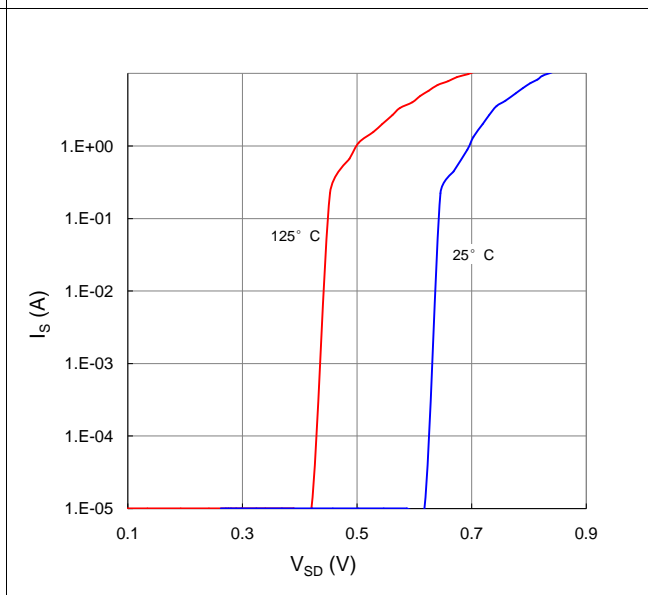


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

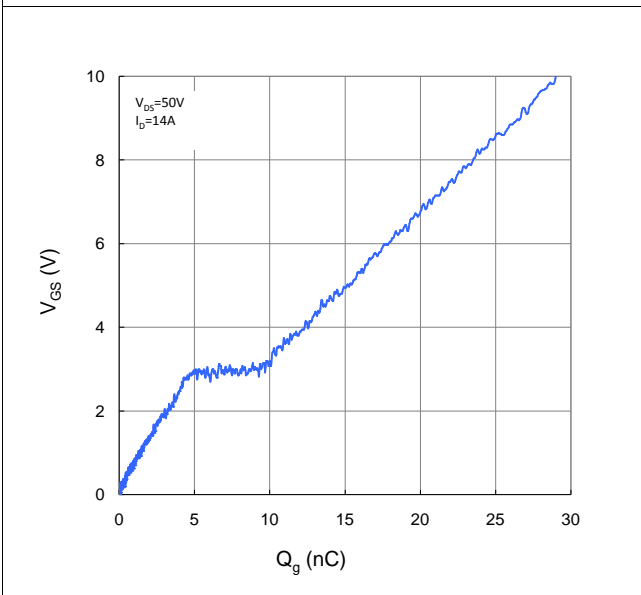


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

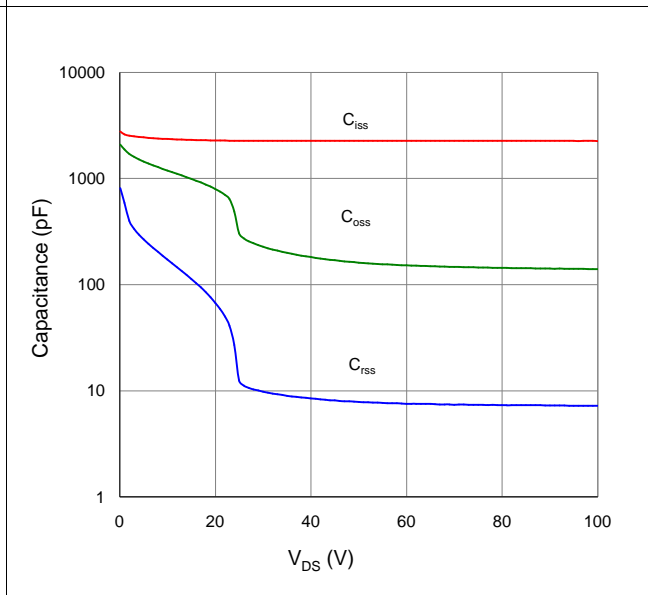


Figure 9. Maximum Safe Operating Area

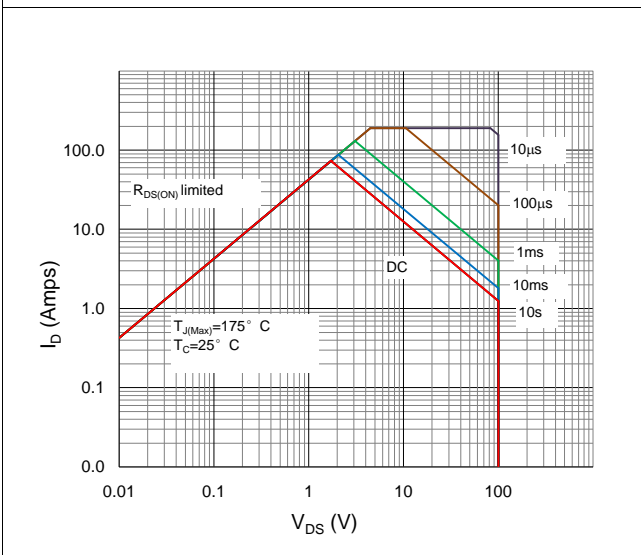


Figure 10. Maximum Drain Current vs. Case Temperature

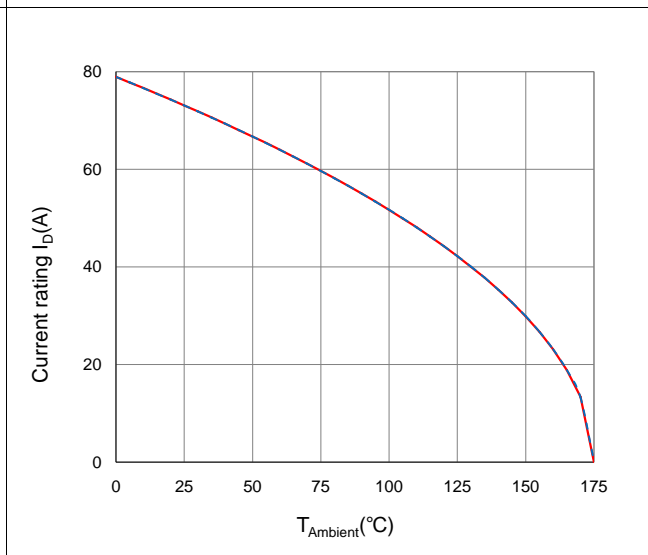
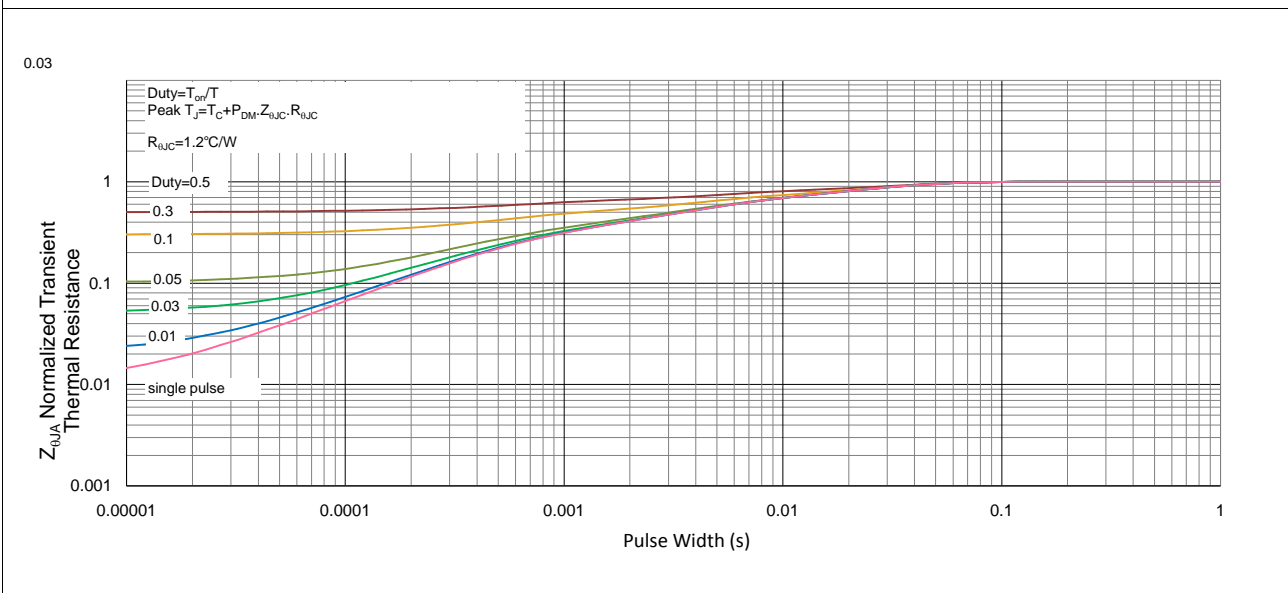
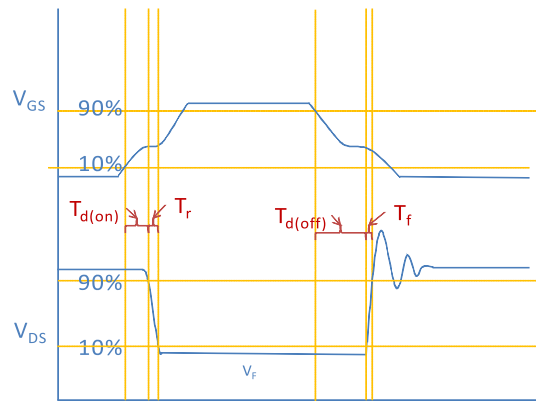
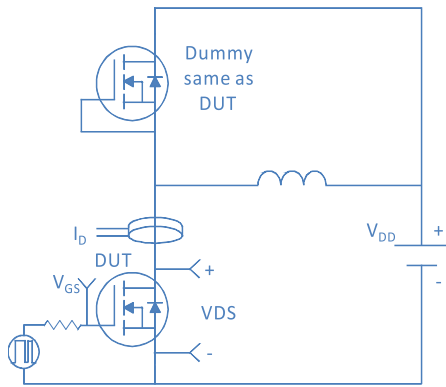


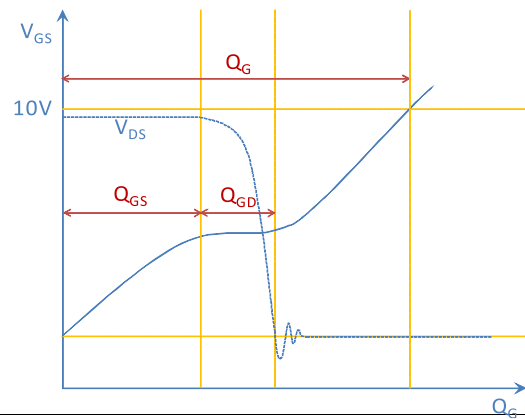
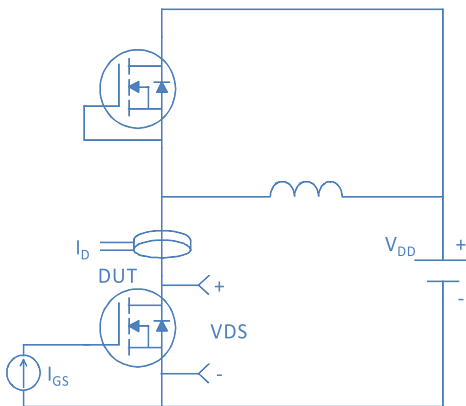
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



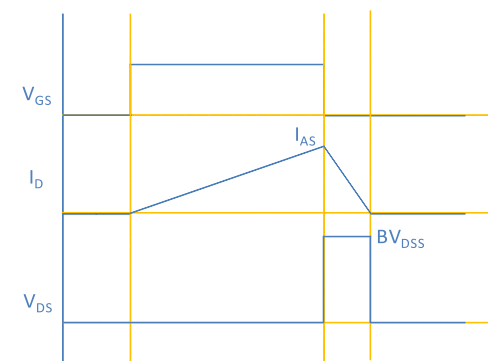
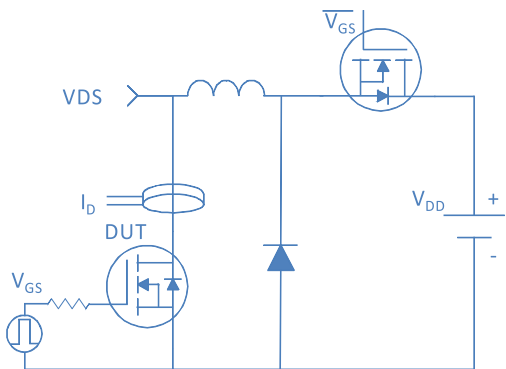
### Inductive switching Test



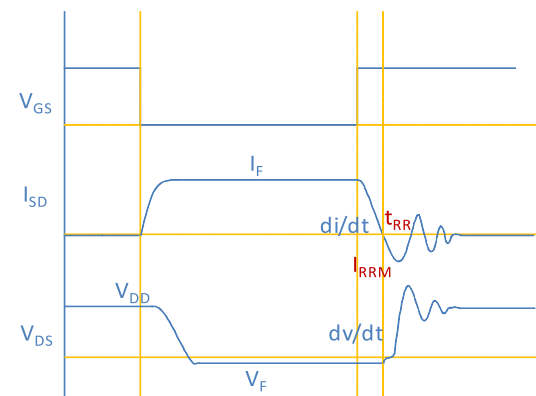
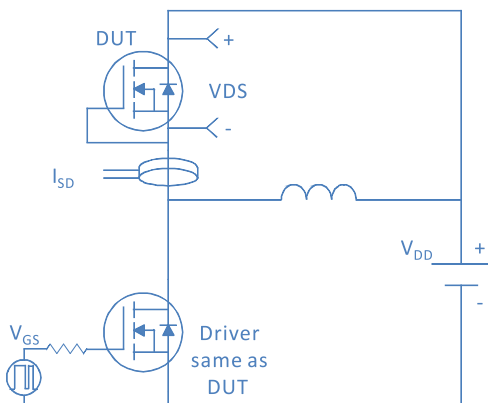
### Gate Charge Test



### Uclamped Inductive Switching (UIS) Test



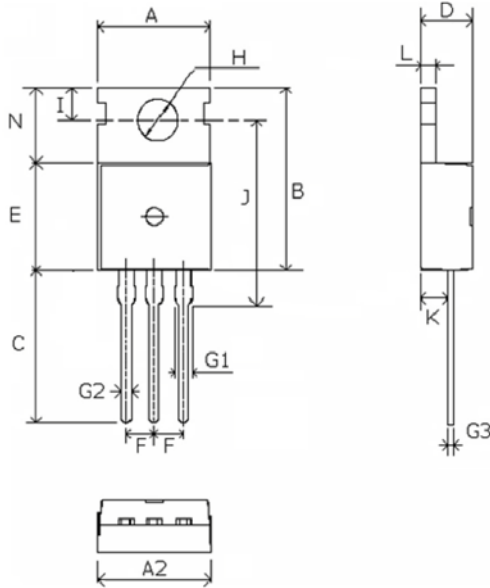
### Diode Recovery Test



Package Outline

TO-220, 3 leads

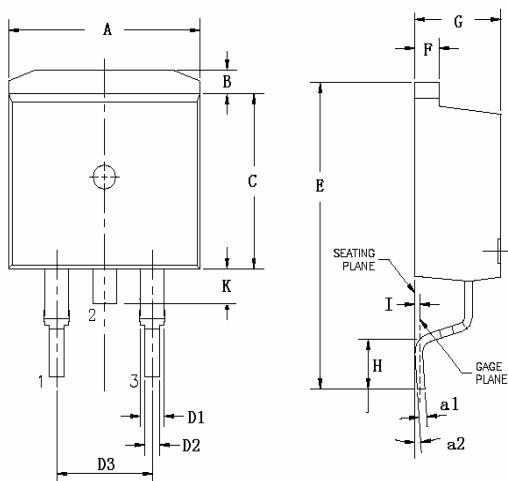
Dimensions in mm unless otherwise specified



Symbol	Min	Nom	Max
A	9.66	9.97	10.28
A2	9.80	10.00	10.20
B	15.60	15.70	15.80
C	12.70	13.48	14.27
D	4.30	4.50	4.70
E	9.00	9.20	9.40
F		2.54	
G1	1.32	1.52	1.72
G2	0.70	0.82	0.95
G3	0.45	0.52	0.60
H	3.50	3.60	3.70
I	2.70	2.80	2.90
J	15.70	15.97	16.25
K	2.20	2.40	2.60
L	1.15	1.27	1.40
N	6.40	6.60	6.80

TO-263, 2 leads

Dimensions in mm unless otherwise specified



Symbol	Min	Nom	Max
A	9.66	9.97	10.28
B	1.02	1.17	1.32
C	8.59	9.00	9.40
D1	1.14	1.27	1.40
D2	0.70	0.83	0.95
D3		5.08	
E	15.09	15.24	15.39
F	1.15	1.28	1.40
G	4.30	4.50	4.70
H	2.29	2.54	2.79
I		0.25	
K	1.30	1.45	1.60
a1	0.45	0.55	0.65
a2(degree)	0°		8°